XC17000 Family of Serial Configuration PROMs

Preliminary Product Specifications

Features

- Extended family of one-time programmable (OTP) bit-serial read-only memories used for storing the configuration bitstreams of Xilinx FPGAs
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions, (the older XC1736A has active-High reset only)
- XC17128 supports XC4000 fast configuration mode (10 MHz)
- Low-power CMOS EPROM process
- Available in 5 V and 3.3 V versions
- Available in plastic and ceramic packages, and commercial, industrial and military temperature ranges
- Space efficient 8-pin DIP, 8-pin SOIC or 20-pin surface-mount packages.
- Programming support by leading programmer manufacturers.

Description

The XC17000 family of serial configuration PROMs (SCPs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in master serial mode, it generates a configuration clock that drives the SCP. A short access time after the rising clock edge, data appears on the SCP DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SCP. When the FPGA is in slave mode, the SCP and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SCPs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, the XACT development system compiles the LCA design file into a standard Hex format, which is then transferred to the programmer.

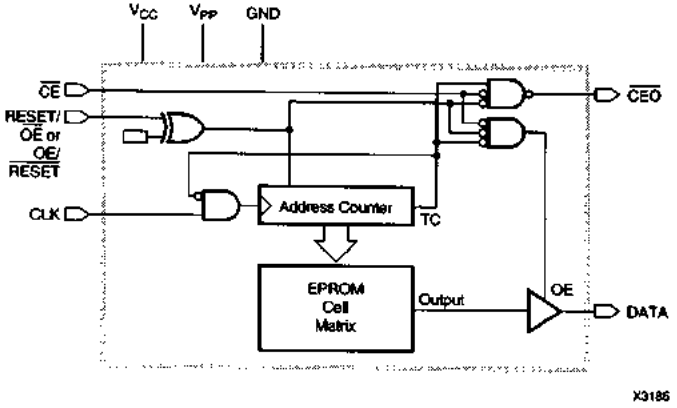


Figure 1. Simplified Block Diagram (does not show programming circuit)

Pin Assignments

DATA
Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK
Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

RESET/$\overline{OE}$
When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/RESET. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices except the older XC1736A.

$\overline{CE}$
When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$
Chip Enable output, to be connected to the CE input of the next SCP in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}
Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave V_{PP} floating!*

V_{CC}
Positive supply pin.

GND
Ground pin

Serial PROM Pinouts

Pin Name	8-Pin	20-Pin
DATA	1	2
CLK	2	4
RESET/$\overline{OE}$ (OE/RESET)	3	6
$\overline{CE}$	4	8
GND	5	10
$\overline{CEO}$	6	14
V_{PP}	7	17
V_{CC}	8	20

Capacity

Device	Configuration Bits
XC1718D or L	18,144
XC1736D or L	36,288
XC1765D or L	65,536
XC17128	131,072

plus 32 bits for reset polarity control

Number of Configuration Bits, Including Header for all Xilinx FPGAs and Compatible SCP Type

Device	Configuration Bits	SCP
XC2064	12,038	XC1718
XC2018	17,878	XC1718
XC3020/3120	14,819	XC1718
XC3030/3130	22,216	XC1736
XC3042/3142	30,824	XC1736
XC3064/3164	46,104	XC1765
XC3090/3190	64,200	XC1765
XC3195	94,984	XC17128
XC4002A	31,668	XC1736
XC4003A	45,676	XC1765
XC4003H	53,967	XC1765
XC4004A	62,244	XC1765
XC4005A	81,372	XC17128
XC4005/4005H	95,000	XC17128
XC4006	119,832	XC17128
XC4008	147,544	XC17128 + XC1718
XC4010	178,136	XC17128 + XC1765
XC4013	247,960	XC17128 + XC17128
XC4025	422,168	XC17128 + XC17128 + XC17128 + XC1736

Controlling Serial PROMs

Most connections between the LCA device and the Serial PROM are simple and self-explanatory.

- The DATA output of the PROM drives DIN of the LCA devices.
- The master LCA CCLK output drives the CLK input of the Serial PROM.
- The $\overline{CEO}$ output of any Serial PROM can be used to drive the $\overline{CE}$ input of the next serial PROM in a cascade chain of PROMs.
- V_{PP} ***must*** be connected to V_{CC}. Leaving V_{PP} open can lead to unreliable, temperature-dependent operation.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$.

1. The LCA D/$\overline{P}$ or LDC output drives both $\overline{CE}$ and $\overline{OE}$ in parallel. This is the simplest connection, but it fails if a user applies $\overline{RESET}$ during the LCA configuration process. The LCA device aborts the configuration and then restarts a new configuration, as intended, but the Serial PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the LCA device is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and D/$\overline{P}$ goes High. However, the LCA configuration will be completely wrong, with potential contentions inside the LCA device and on its output pins. *This method must, therefore, never be used when there is any chance of external reset during configuration.*

PRELIMINARY

2. The LCA D/$\overline{P}$ or LDC output drives only the $\overline{CE}$ input of the Serial PROM while its $\overline{OE}$ input is driven by the LCA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. The Low level on the OE input during reset clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. The reset polarity should be inverted for this mode to be used. It is strongly recommended that this method, shown in Figure 2, be used whenever possible.

LCA Master Serial Mode Summary

The I/O and logic functions of the Logic Cell Array and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three LCA mode pins. In Master Mode, the Logic Cell Array automatically loads the configuration program from an external memory. The Serial Configuration PROM has been designed for compatibility with the Master Serial Mode.

Upon power-up or reconfiguration, an LCA device enters the Master Serial Mode whenever all three of the LCA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an LCA device. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the LCA device is used only for configuration, it must still be held at a defined level during normal operation. The XC3000 and XC4000 families take care of this automatically with an on-chip default pull-up resistor. With XC2000-family devices, the user must either configure DIN as an active output, or provide a defined level, e.g., by using an external pull-up resistor, if DIN is configured as an input.

Programming the LCA With Counters Unchanged Upon Completion

When multiple LCA-configurations for a single LCA are stored in a Serial Configuration PROM, the $\overline{OE}$ pin should be tied Low as shown in Figure 3. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the LCA with another program, the D/$\overline{P}$ line is pulled Low and configuration begins at the last value of the address counters.

Cascading Serial Configuration PROMs

For multiple LCAs configured as a daisy-chain, or for future LCAs requiring larger configuration memories, cascaded SCPs provide additional memory. After the last bit from the first SCP is read, the next clock signal to the SCP asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SCP recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SCPs are reset if the LCA $\overline{RESET}$ pin goes Low, assuming the SCP reset polarity option has been inverted.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground, as shown in Figure 3. To reprogram the LCA device with another program, the D/$\overline{P}$ line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

When more than a few SCPs are daisy-chained, the designer must evaluate the worst-case CCLK-to-DATA delay resulting from the cascaded $\overline{CE}$-to-$\overline{CEO}$ delays. All Xilinx LCA devices require valid input data a set-up time before the next rising CCLK edge.

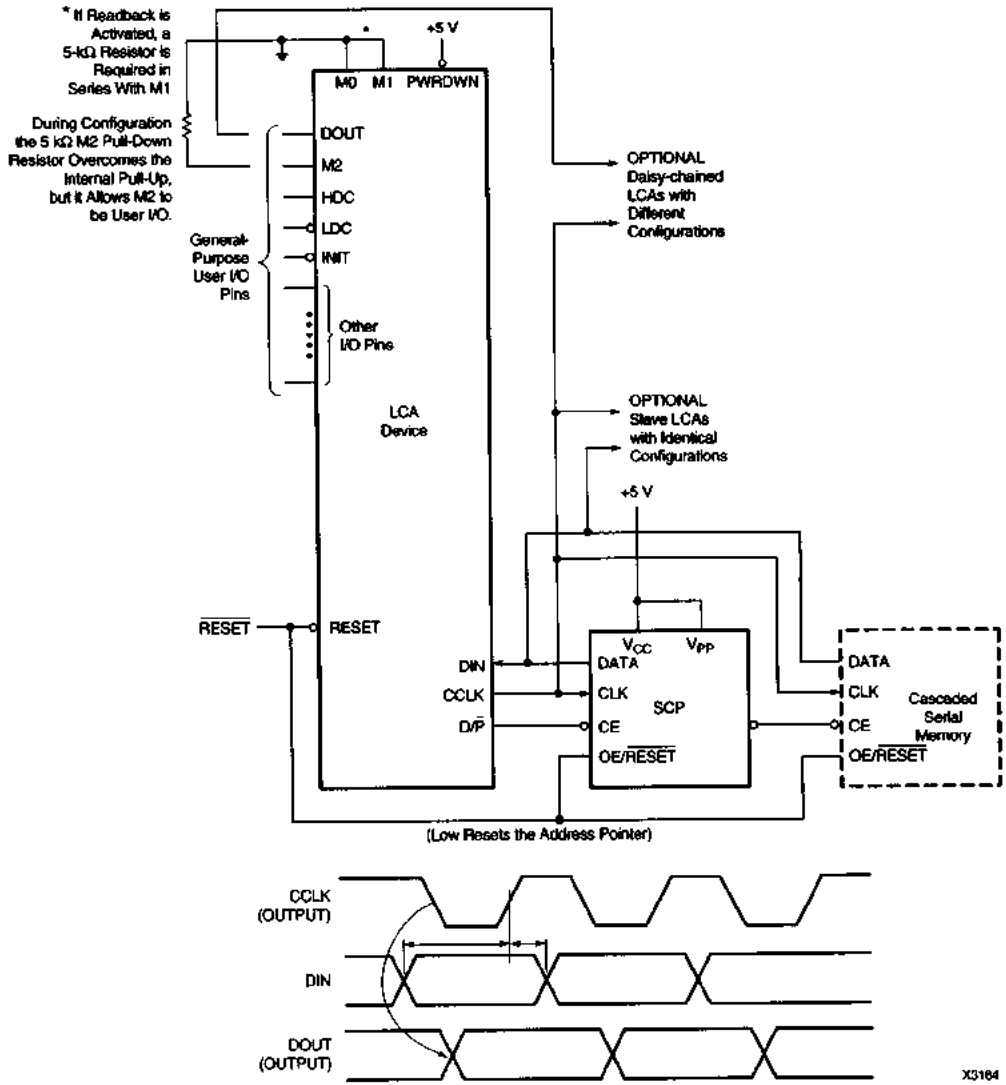
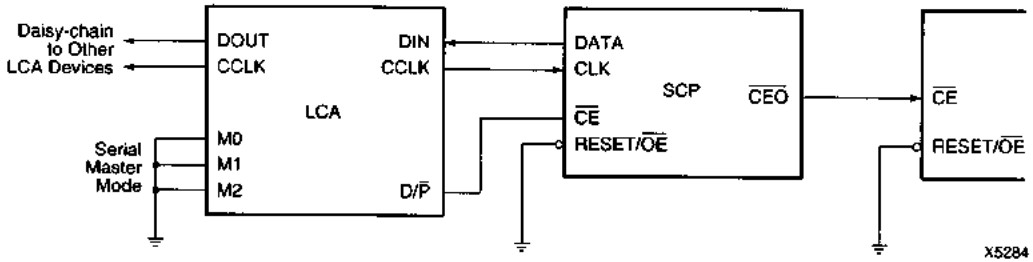


Figure 2. Master Serial Mode. The one-time-programmable Serial Configuration PROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional LCA devices. An early D/$\overline{P}$ inhibits the PROM data output one CCLK cycle before the LCA I/Os become active.



Notes: 1. If programmed for active High Reset, tie RESET to V_{CC}.
2. If M2 is tied directly to ground, it should be programmed as an input during operation.
3. If the LCA is reset during configuration, it will abort back to initialization state. An external signal is then required to reset the XC17XX counters.

Figure 3. Address Counters Not Reset at the End of Configuration

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the SCP consumes less than 0.5 mA of current. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Reducing Standby Current to Zero

The 0.5 mA of serial PROM standby current may be unacceptable in a low-current application. It is, however, possible to achieve zero standby current by disconnecting the PROM ground lead from system ground and connecting it to the $\overline{LDC}$ pin of the LCA, as shown in Figure 4.

As a result, the PROM powers up together with the LCA, since $\overline{LDC}$ goes Low immediately after power-up; the PROM then stays powered-up until the end of the configuration process. When the user outputs go active, $\overline{LDC}$ must go 3-state and thus cut off the PROM supply current. $\overline{LDC}$ must, therefore, be configurated as an input with pull-up resistor, not as an active High output.

The PROM operating current (typically <5 mA) causes a voltage drop of typically 100 mV on the $\overline{LDC}$ output, reducing the PROM supply voltage by that amount. This violates the specification, but is guaranteed to work, since all PROMs are factory-tested at 4.5 V V_{CC}. Multiple PROMs increase the $\overline{LDC}$ sink current by only 0.5 mA per additional PROM.

$\overline{LDC}$ must never be active High, because there might be a few more CCLK pulses at the end of configuration, which will pull the PROM's CLK input below the level of the PROM ground pin. In user mode, it is, therefore, important to avoid driving the PROM with any active High or Low levels. That means that the $\overline{LDC}$ and DIN pins cannot be used in user mode, they must both be configurated as inputs with a pull-up resistor. The $\overline{CE}$ input must be tied to the SCP ground pin. $\overline{RESET}$ (active Low) must be connected to the LCA $\overline{RESET}$ input.

This design assumes that only one configuration bitstream is stored in one or multiple PROMs. It is inherently impossible to use this design when multiple bitstreams are stored in one PROM or one daisy chain of PROMs.

Programming the XC17000 Family Serial PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and voltage are used. Different product types use different algorithms and voltages, and the wrong choice can permanently damage the device.

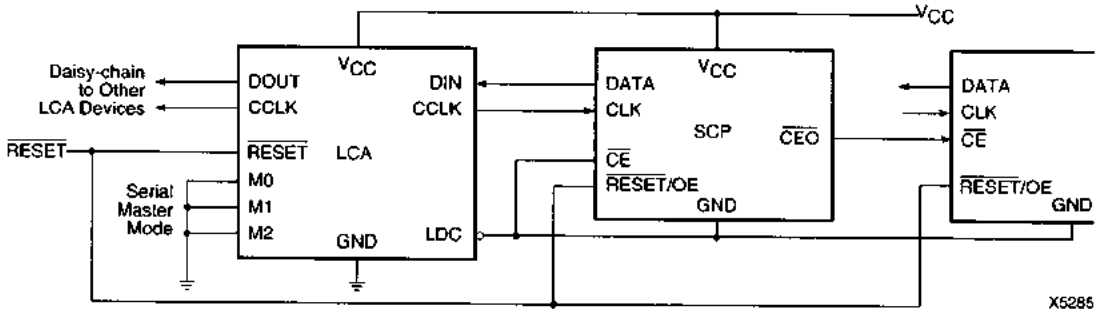


Figure 4. Zero-Standby Current Circuit

XC1718D, XC1736D, XC1765D, XC17128

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND: XC1718D, XC1736D, XC1765D	-0.5 to +12.5	V
	Supply voltage relative to GND: XC17128	-0.5 to +15.5	V
V_{IN}	Input voltage relative to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0 °C to +70°C	4.75	5.25	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	V

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)	Commercial		0.32	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)	Industrial		0.37	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)	Military		0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_{CCS}	Supply current, standby mode			0.5	mA
I_L	Input or output leakage current		-10	10	µA

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

XC1718L and XC1765L

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +6.0	V
V_{PP}	Supply voltage relative to GND	-0.5 to +12.5	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

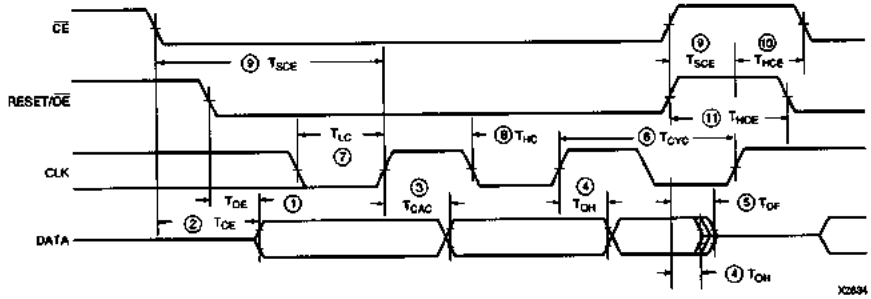
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0 °C to +70°C	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	3.0	3.6	V

DC Characteristics Over Operating Condition

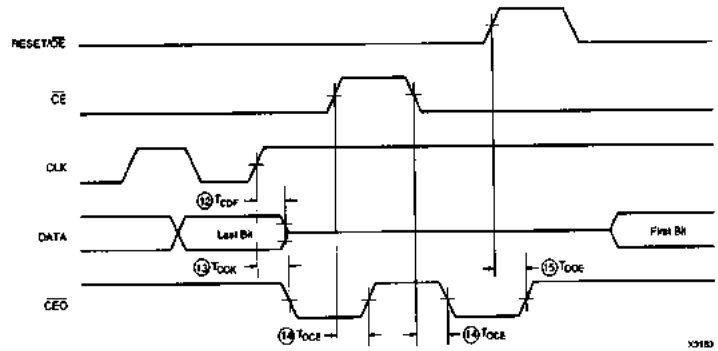
Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = -4 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		0.4	V
I_{CCA}	Supply current, active mode		5	mA
I_{CCS}	Supply current, standby mode		0.5	mA
I_L	Input or output leakage current	-10	10	µA

Note: During normal read operation V_{PP} ***must*** be connected to V_{CC}

AC Characteristics Over Operating Conditions



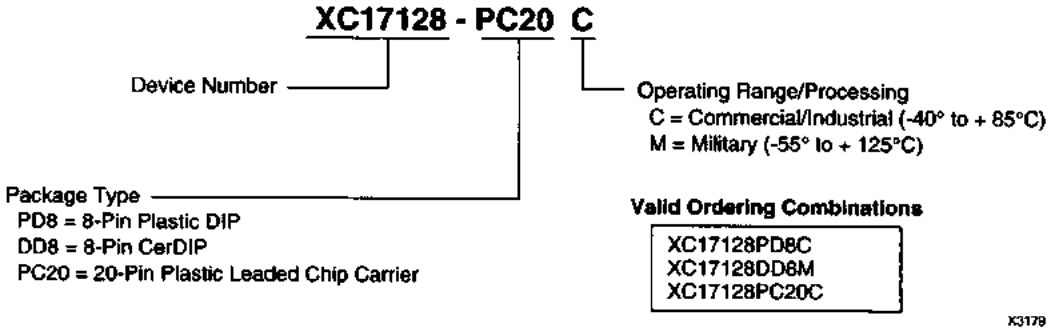
Symbol		Description	XC1718D, XC1736D, XC1765D		XC1718L, XC1765L		XC17128		Units
			Min	Max	Min	Max	Min	Max	
1	T_{HOE}	$\overline{OE}$ to Data Delay		45		45		50	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60		60		50	ns
3	T_{CAC}	CLK to Data Delay		150		200		60	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		0		0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay[2]		50		50		50	ns
6	T_{CYC}	Clock Periods	200		400		100		ns
7	T_{LC}	CLK Low Time[3]	100		100		25		ns
8	THC	CLK High Time[3]	100		100		25		ns
9	TSCE	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		40		25		ns
10	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		0		0		ns
11	T_{HOE}	$\overline{OE}$ High Time (guarantees counters are reset)	100		100		20		n

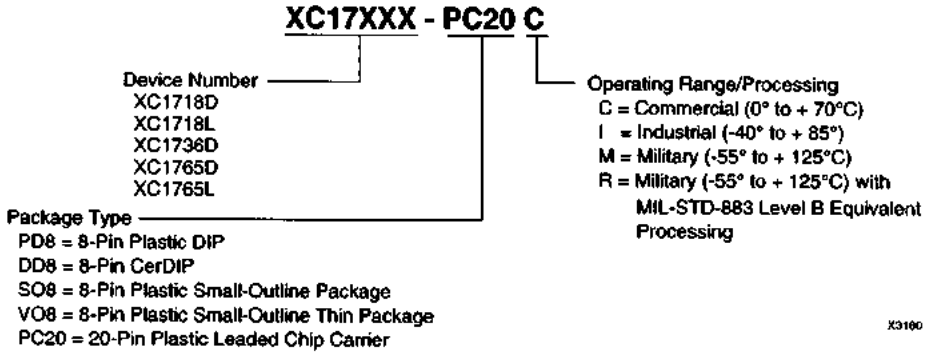


Symbol		Description	XC1718D, XC1736D, XC1765D		XC1718L, XC1765L		XC17128		Units
			Min	Max	Min	Max	Min	Max	
12	T_{CDF}	CLK to Data Float Delay[2]		50		50		50	ns
13	T_{OCK}	CLK to $\overline{CEO}$ Delay		65		65		40	ns
14	T_{OCE}	CE to $\overline{CEO}$ Delay		45		45		40	ns
15	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40		40		45	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with minimum tester ac load and maximum dc load.
3. Guaranteed by design, not tested.
4. All ac parameters are measured with V_{IL} = 0.0 V and V_{IH} = 3.0 V.

Ordering Information





Valid Ordering Combinations

XC1718DPD8C XC1718DPD8I XC1718DSO8C XC1718DVO8C XC1718DSO8I XC1718DVO8I XC1718DPC20C XC1718DPC20I	XC1736DPD8C XC1736DPD8I XC1736DSO8C XC1736DVO8C XC1736DSO8I XC1736DVO8I XC1736DPC20C XC1736DPC20I XC1736DDD8M	XC1765DPD8C XC1765DPD8I XC1765DSO8C XC1765DVO8C XC1765DSO8I XC1765DVO8I XC1765DPC20C XC1765DPC20I XC1765DDD8M XC1765DDD8R	XC1718LPD8C XC1718LSO8C XC1718LVO8C XC1718LPC20C	XC1765LPD8C XC1765LSO8C XC1765LVO8C XC1765LPC20C

X3181

Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.