

DRAM MODULE

1 MEG x 8

1 MEGABYTE, 5V,
FAST PAGE MODE

FEATURES

- JEDEC- and industry-standard pinout in a 30-pin, single-in-line memory module (SIMM)
- High-performance CMOS silicon-gate process
- Single 5V $\pm 10\%$ power supply
- Low power, 6mW standby; 450mW active, typical
- All device pins are TTL-compatible
- FAST PAGE MODE (FPM) access cycle
- Refresh modes: RAS ONLY, CAS-BEFORE-RAS (CBR) and HIDDEN
- Low profile
- 1,024-cycle refresh distributed across 16ms

OPTIONS

- Timing
 - 60ns access
 - 70ns access

MARKING

-6
-7

- Packages
 - 30-pin SIMM

M

- Part Number Example: MT2D18M-6

KEY TIMING PARAMETERS

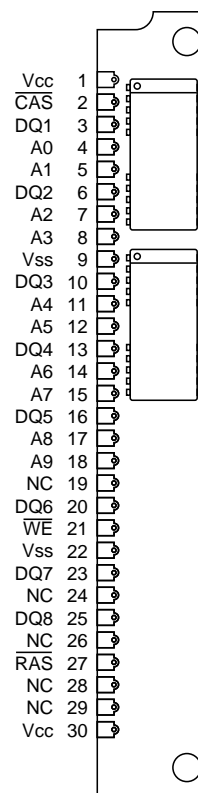
SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

GENERAL DESCRIPTION

The MT2D18 is a randomly accessed solid-state memory containing 1,048,576 words organized in a x8 configuration. During READ or WRITE cycles, each word is uniquely addressed through 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ or WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. Early WRITE occurs when WE goes LOW prior to CAS going LOW, and the output pins remain open (High-Z) until the next CAS cycle.

PIN ASSIGNMENT (Front View)

30-Pin SIMM (DD-1)



FAST PAGE MODE

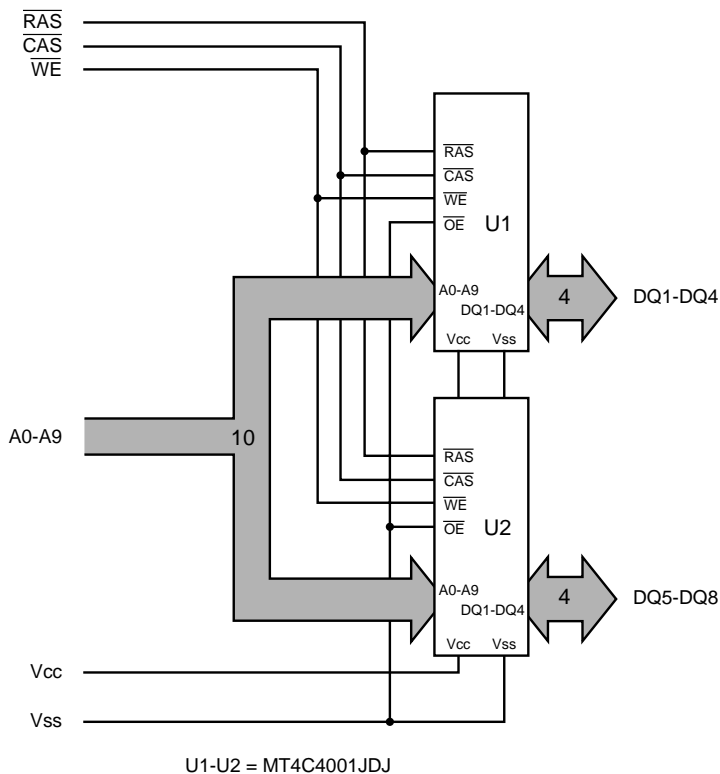
FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles.

REFRESH

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any

$\overline{\text{RAS}}$ cycle (READ, WRITE) or $\overline{\text{RAS}}$ refresh cycle ($\overline{\text{RAS}}$ ONLY, CBR or HIDDEN) so that all 1,024 combinations of $\overline{\text{RAS}}$ addresses (A0-A9) are executed at least every 16ms regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDRESSES		DATA-IN/OUT
					t_R	t_C	DQ1-DQ8
Standby		H	H→X	X	X	X	High-Z
READ		L	L	H	ROW	COL	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	n/a	COL	Data-Out
FAST-PAGE-MODE WRITE	1st Cycle	L	H→L	L	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	n/a	COL	Data-In
$\overline{\text{RAS}}$ -ONLY REFRESH		L	H	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1V to +7V
 Operating Temperature, T_A (ambient) 0°C to +70°C
 Storage Temperature -55°C to +125°C
 Power Dissipation 2W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V _{IH}	2.4	V _{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	0.8	V	
INPUT LEAKAGE Any input 0V ≤ V _{IN} ≤ 6.5V (All other pins not under test = 0V)	I _I	-4	4	μA	A0-A9, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$
OUTPUT LEAKAGE (Q is disabled; 0V ≤ V _{OUT} ≤ 5.5V)	I _{OZ}	-10	10	μA	DQ1-DQ8
OUTPUT LEVELS Output High (Logic 1) Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low (Logic 0) Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-6	-7		
STANDBY CURRENT: (TTL) ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$)	I _{CC1}	4	4	mA	
STANDBY CURRENT: (CMOS) ($\overline{\text{RAS}} = \overline{\text{CAS}} = \text{Other Inputs} = V_{CC} - 0.2V$)	I _{CC2}	2	2	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: t _{RC} = t _{RC} [MIN])	I _{CC3}	220	200	mA	2, 26, 28
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, Address Cycling: t _{PC} = t _{PC} [MIN])	I _{CC4}	160	140	mA	2, 26, 28
REFRESH CURRENT: $\overline{\text{RAS}}$ ONLY Average power supply current ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$: t _{RC} = t _{RC} [MIN])	I _{CC5}	220	200	mA	26, 28
REFRESH CURRENT: CBR Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: t _{RC} = t _{RC} [MIN])	I _{CC6}	220	200	mA	19, 26

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C _{I1}		13	pF	17
Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	C _{I2}		17	pF	17
Input/Output Capacitance: DQ1-DQ8	C _{I0}		10	pF	17

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 3, 4, 5, 6, 7, 10, 11, 16) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	t_{AA}		30		35	ns	
Column-address hold time (referenced to $\overline{\text{RAS}}$)	t_{AR}	45		50		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Access time from $\overline{\text{CAS}}$	t_{CAC}		15		20	s	9
Column-address hold time	t_{CAH}	10		15		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ hold time (CBR REFRESH)	t_{CHR}	10		10		ns	19
$\overline{\text{CAS}}$ to output in Low-Z	t_{CLZ}	0		0		ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	10		10		ns	18
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}		35		40	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	10		10		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	60		70		ns	
$\overline{\text{CAS}}$ setup time (CBR REFRESH)	t_{CSR}	10		10		ns	19
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	10		15		ns	15
Data-in hold time (referenced to $\overline{\text{RAS}}$)	t_{DHR}	45		55		ns	
Data-in setup time	t_{DS}	0		0		ns	15
Output buffer turn-off delay	t_{OFF}	3	15	3	20	ns	12, 27
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	n/a		n/a		n/a	21
Access time from $\overline{\text{RAS}}$	t_{RAC}		60		70	ns	8
$\overline{\text{RAS}}$ to column-address delay time	t_{RAD}	15	30	15	35	ns	22
Row-address hold time	t_{RAH}	10		10		ns	
Column-address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30		35		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

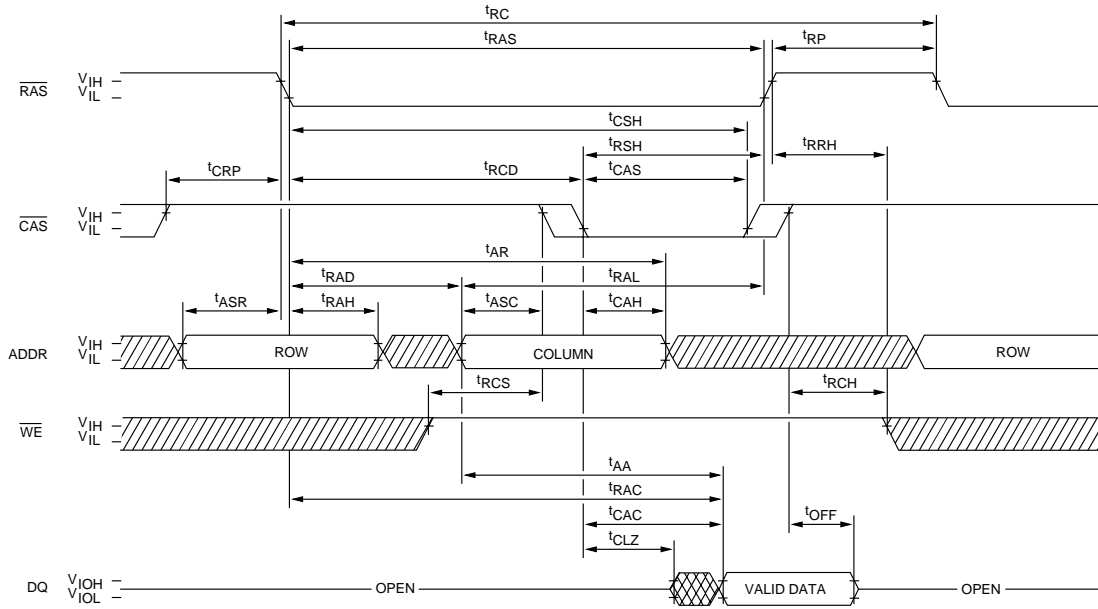
 (Notes: 3, 4, 5, 6, 7, 10, 11, 16, 21) ($V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	ns	13
Read command hold time (referenced to \overline{CAS})	t_{RCH}	0		0		ns	24
Read command setup time	t_{RCS}	0		0		ns	
Refresh period (1,024 cycles)	t_{REF}		16		16	ms	
\overline{RAS} precharge time	t_{RP}	40		50		ns	
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	0		0		ns	
Read command hold time (referenced to \overline{RAS})	t_{RRH}	0		0		ns	24
\overline{RAS} hold time	t_{RSH}	15		20		ns	
READ WRITE cycle time	t_{RWC}	n/a		n/a		n/a	21
Write command to \overline{RAS} lead time	t_{RWL}	15		20		ns	
Transition time (rise or fall)	t_T	3	50	3	50	ns	
Write command hold time	t_{WCH}	10		15		ns	
Write command hold time (referenced to \overline{RAS})	t_{WCR}	45		55		ns	
\overline{WE} command setup time	t_{WCS}	0		0		ns	
Write command pulse width	t_{WP}	10		15		ns	
\overline{WE} hold time (CBR REFRESH)	t_{WRH}	10		10		ns	23
\overline{WE} setup time (CBR REFRESH)	t_{WRP}	10		10		ns	23

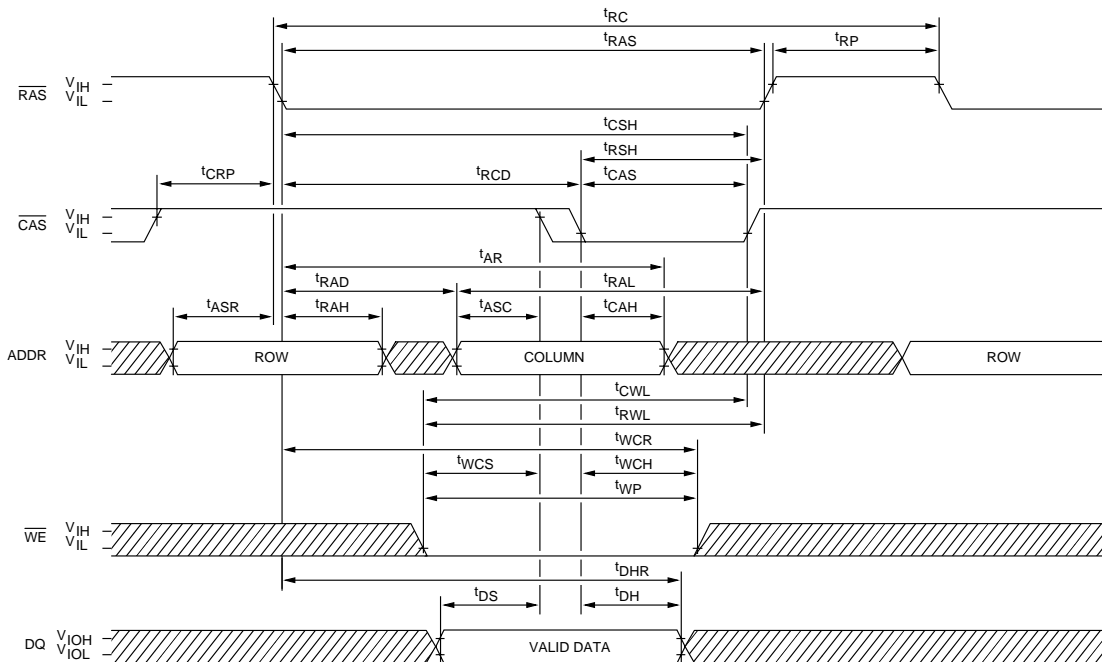
NOTES



1. All voltages referenced to V_{SS} .
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
3. An initial pause of $100\mu s$ is required after power-up followed by any eight \overline{RAS} refresh cycles (\overline{RAS} ONLY or CBR with \overline{WE} HIGH) before proper device operation is assured. The eight \overline{RAS} cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
4. AC characteristics assume $t_T = 5ns$.
5. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^\circ C \leq T_A \leq 70^\circ C$) is assured.
7. Measured with a load equivalent to two TTL gates and $100pF$.
8. Assumes that $t_{RCD} < t_{RCD} (MAX)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD} (MAX)$.
10. If $\overline{CAS} = V_{IH}$, data output is High-Z.
11. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
12. $t_{OFF} (MAX)$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
13. Operation within the $t_{RCD} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RCD} (MAX)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (MAX)$ limit, then access time is controlled exclusively by t_{CAC} .
14. t_{RCH} is referenced to the first rising edge of \overline{RAS} or \overline{CAS} .
15. These parameters are referenced to \overline{CAS} leading edge in EARLY WRITE cycles.
16. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, $V_{CC} = 5V$, DC bias = $2.4V$ at $15mV$ RMS).
18. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , data-out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, \overline{CAS} must be pulsed HIGH for t_{CP} .
19. On-chip refresh and address counters are enabled.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE} = LOW$.
21. LATE WRITE, READ WRITE or READ-MODIFY-WRITE cycles are not available due to \overline{OE} being grounded on U1 and U2.
22. Operation within the $t_{RAD} (MAX)$ limit ensures that $t_{RAC} (MIN)$ and $t_{CAC} (MIN)$ can be met. $t_{RAD} (MAX)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (MAX)$ limit, then access time is controlled exclusively by t_{AA} .
23. t_{WTS} and t_{WTH} are setup and hold specifications for the \overline{WE} pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverses of t_{WRP} and t_{WRH} in the CBR REFRESH cycle.
24. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
25. All other inputs at $V_{CC} - 0.2V$.
26. I_{CC} is dependent on cycle rates.
27. The $3ns$ minimum is a parameter guaranteed by design.
28. Column-address changed once each cycle.

READ CYCLE

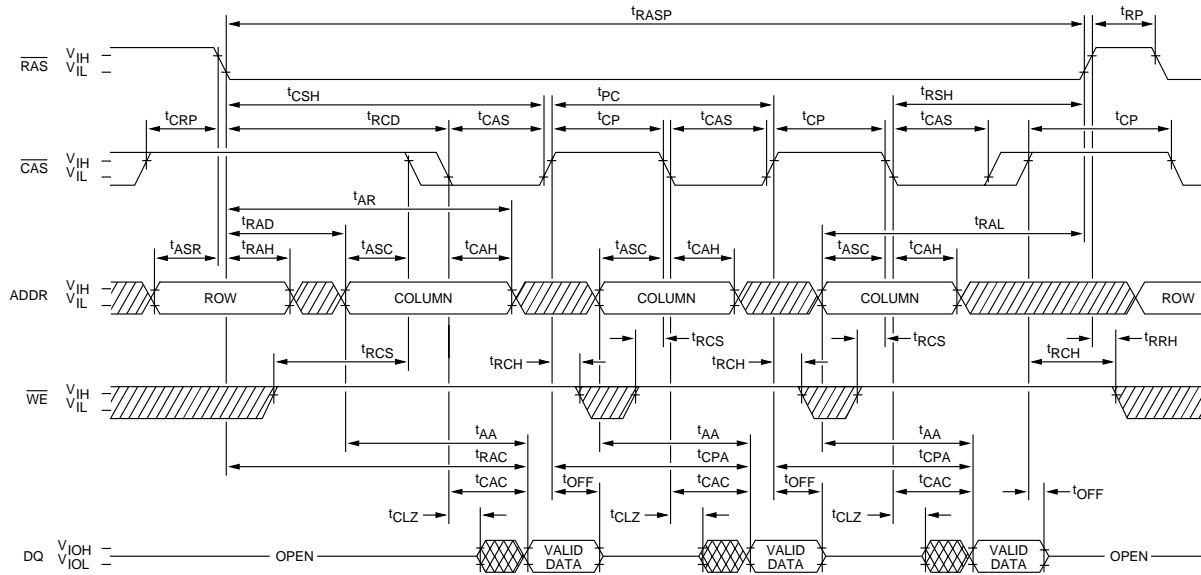


EARLY WRITE CYCLE

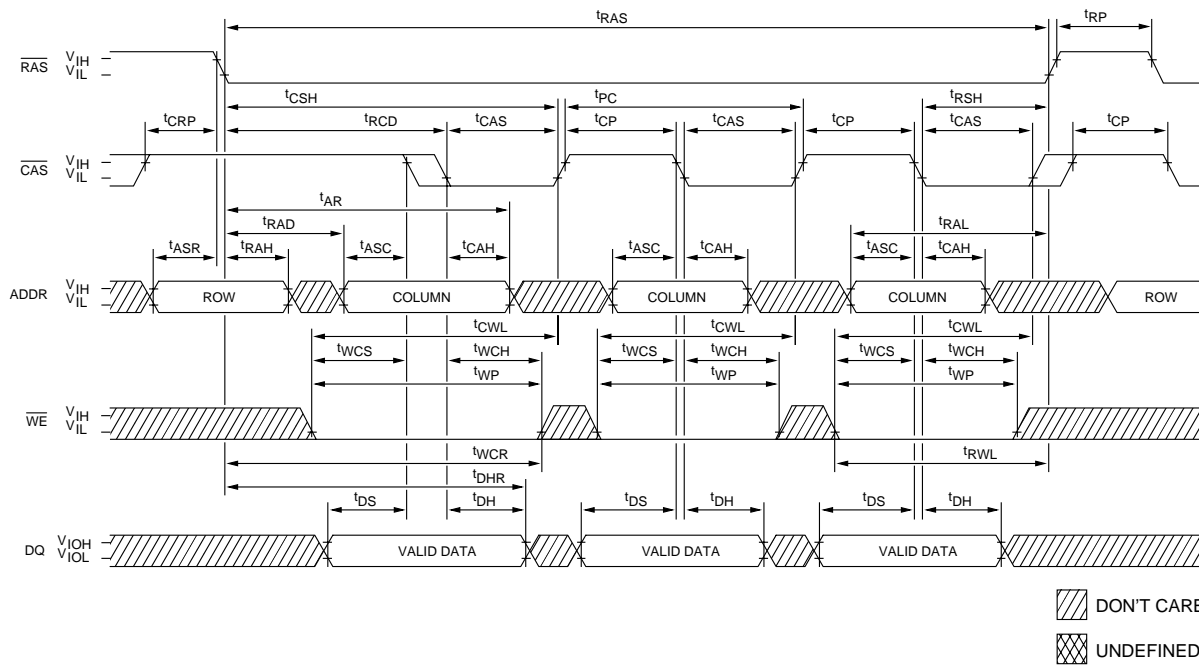




 DON'T CARE
 UNDEFINED

FAST-PAGE-MODE READ CYCLE

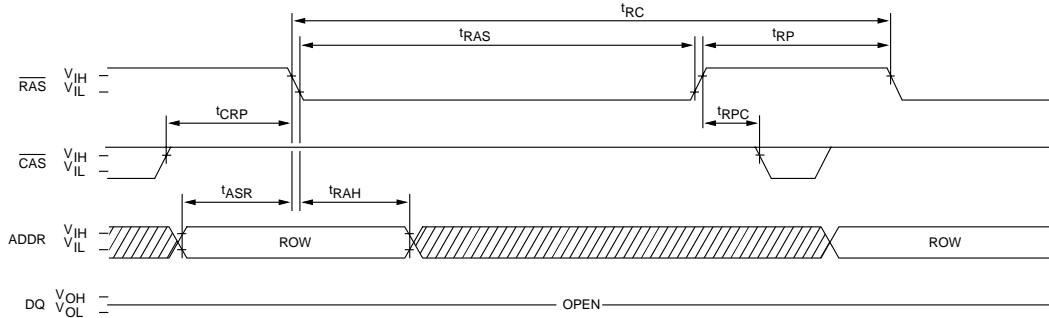


FAST-PAGE-MODE EARLY-WRITE CYCLE

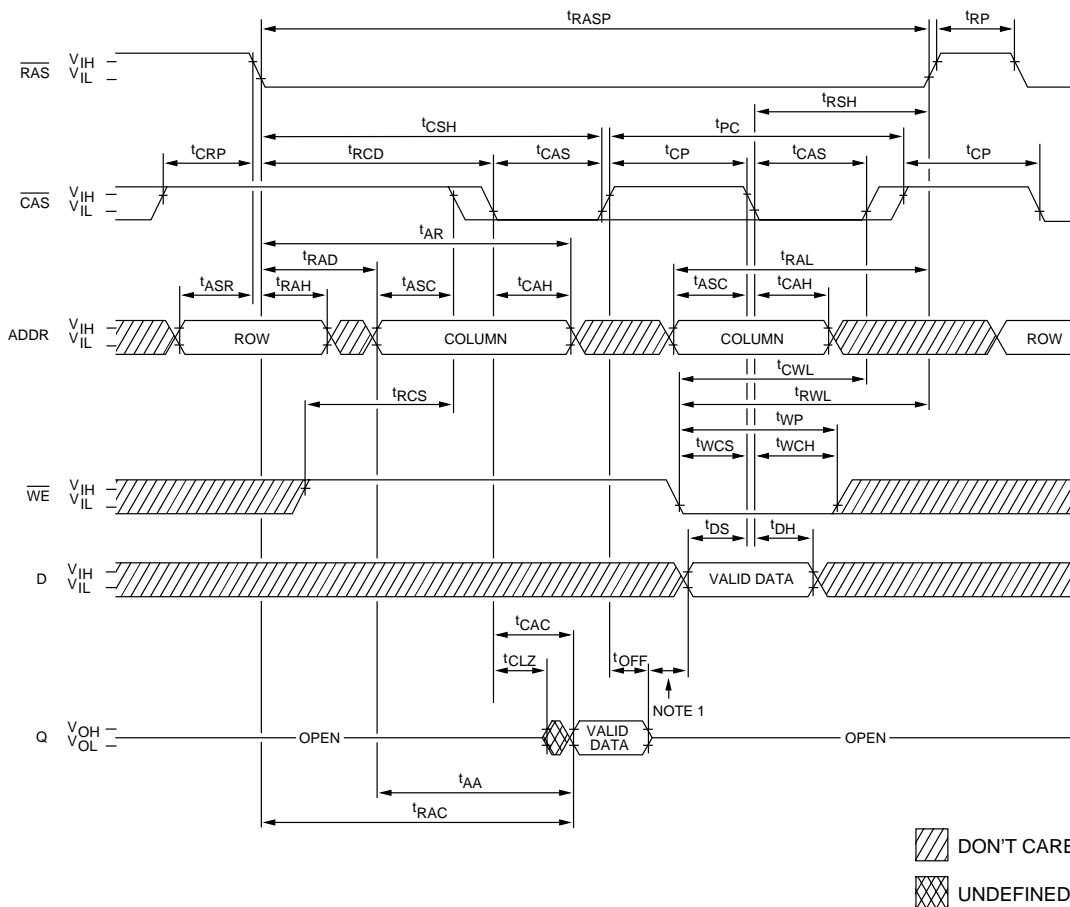


 DON'T CARE
 UNDEFINED

RAS-ONLY REFRESH CYCLE
(WE = DON'T CARE)

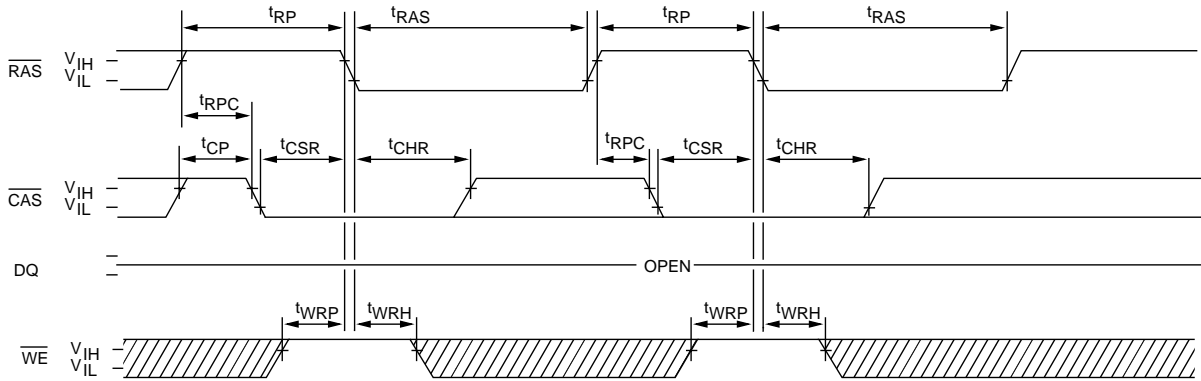


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

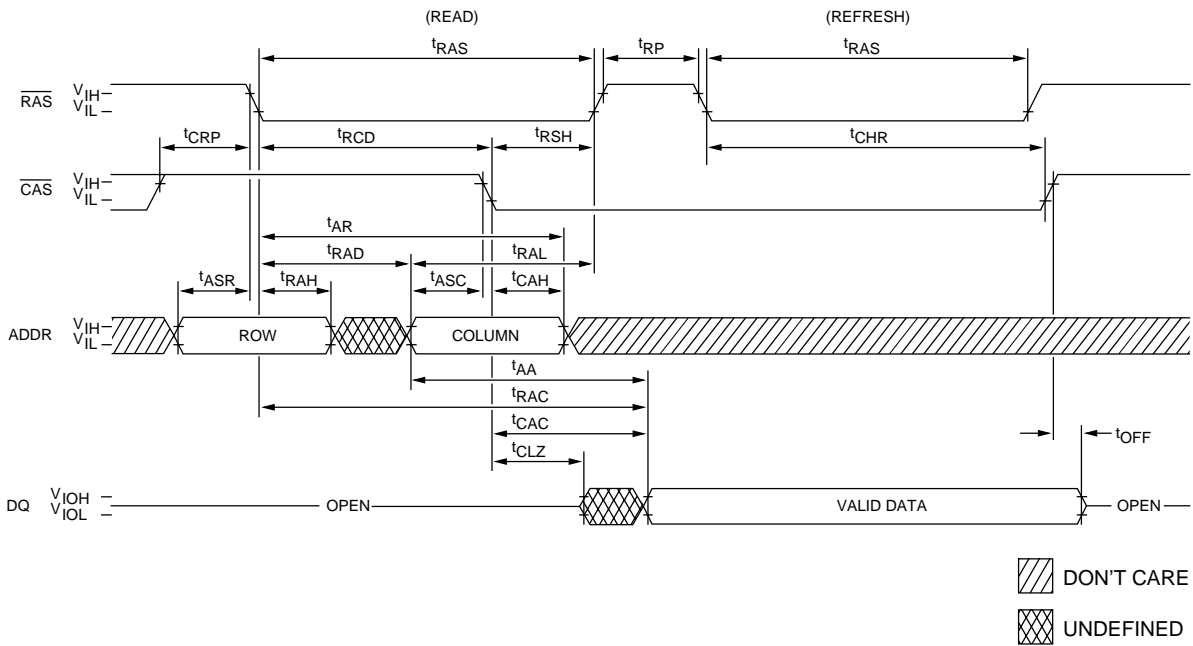


NOTE: 1. Do not drive data prior to tristate.

CBR REFRESH CYCLE
(Addresses = DON'T CARE)



HIDDEN REFRESH CYCLE²⁰
(WE = HIGH)



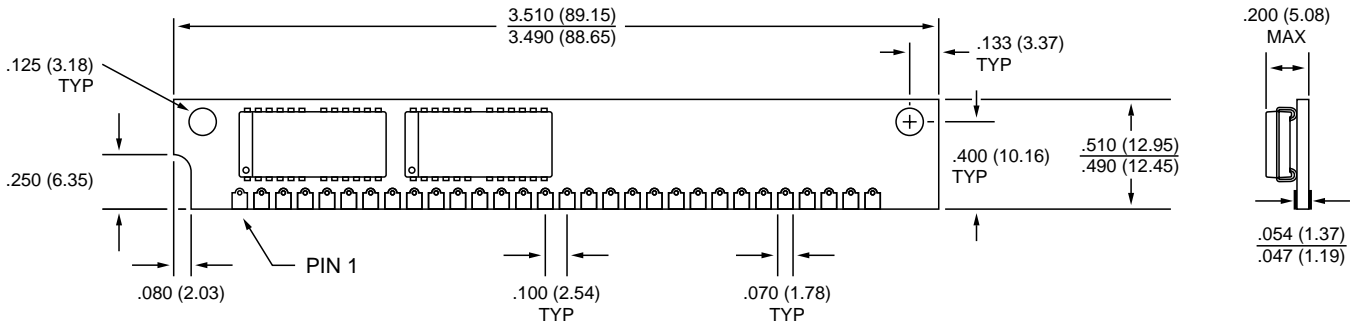
▨ DON'T CARE
▩ UNDEFINED

OBSOLETE



MT2D18 1 MEG x 8 DRAM MODULE

30-Pin SIMM



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmtg@micron.com, Internet: <http://www.micron.com>, Customer Comment Line: 800-932-4992
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